A New Process Technique for Complementary Metal-Oxide-Semiconductor [CMOS] Compatible Sensors

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A new sacrificial-etching-window (SEW) structure is reported for the first time, which can be used for most complementary metal-oxide-semiconductor (CMOS) compatible sensor structures. Using a buried sacrificial layer, the etching windows of the substrate can be extended beneath the membrane. The SEW technique combines the advantages of both surface micromachining by using a sacrificial layer structure and bulk micromachining by anisotropic etching of a silicon substrate. Using the SEW structure, one can speed up the etching rate and design a larger membrane with a larger active area. Several sensors are fabricated by 1.2 $\mu$m industrial CMOS IC technologies combined with subsequent anisotropic front-side etching stops. Three kinds of SEW thermoelectric sensors are reported in this paper, and the characteristics of the sensors are analyzed and measured.

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